REMARKS

Applicants note with appreciation that the Office Action at page 7 indicates that claims 4-6 and 19-20 are allowed, and that claims 10 and 18 would be allowable if rewritten in independent form. New claim 21 is claim 10 rewritten in independent form. New claim 22 is claim 18 rewritten in independent form. Allowance of new claims 21 and 22 is respectfully requested.

Claims 1-3, 11 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Ooishi (U.S. Patent Number 6,519,192). Claims 8, 14, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka (U.S. Patent Number 6,542,428) in view of Ooishi. In view of the amended claims and the following remarks, it is believed that the claims are allowable over the cited reference, and therefore, reconsideration and removal of the rejections are respectfully requested.

Independent claim 1 is amended herein to clarify that Applicants' claimed semiconductor memory device comprises at least one data input pad and at least one data output pad. In addition, claim 1 is amended to clarify that a data input circuit is between the at least one data input pad and a predetermined number of write line pairs for transmitting first data which is applied through the at least one data input pad to the predetermined number of write line pairs as second data during a write operation, and a data output circuit between the at least one output pad and a predetermined number of read line pairs for outputting third data as fourth data during a read operation. In addition, claim 1 is amended herein to clarify that a plurality of write column selection gates receives first data from the data input circuit and transmits the second data between a plurality of bit line pairs and the predetermined number of write line pairs in response to a write column selection signal during a write operation. In addition, claim 1 is amended to clarify that a plurality of read column selection gates transmits third data between the plurality of bit line pairs and the predetermined number of read line pairs in response to a read column selection signal during a read operation. In addition, claim 1 is amended herein to clarify that a data output circuit is between the at least one data output pad and the predetermined number of read line pairs for outputting the third data as fourth data during the read operation, wherein the fourth data is output through the at least one data output pad, and wherein the first data is input

through the at least one data input pad during the write operation and the fourth data is output through the at least one data output pad during the read operation simultaneously.

Independent 8 is amended herein to clarify that Applicants' claimed semiconductor memory device comprises at least one data input pad and at least one data output pad. In addition, independent claim 8 is amended herein to clarify that a plurality of write column selection gates of each of a plurality of memory cell array blocks transmits data between a plurality of bit line pairs and a predetermined number of local write line pairs in response to write column selection signals during a write operation. In addition, claim 8 is amended herein to clarify that read column selection gates of each of the plurality of memory cell array blocks transmits data between the plurality of bit line pairs and a predetermined number of local read line pairs in response to read column selection signals during a read operation. In addition, claim 8 is amended herein to clarify that a data input circuit is between at least one data input pad and a predetermined number of global write line pairs for transmitting data input from the at least one data input pad to the predetermined number of global write line pairs, and a data output circuit is between at least one data output pad and global read line pairs for outputting data transmitted from the predetermined number of global read line pairs to the at least one data output pad. In addition, claim 8 is amended herein to clarify that data transmitted from the at least one data input pad is transmitted during a write operation and the data output to the at least one data output pad is output during a read operation simultaneously.

Independent claim 14 is amended herein to clarify that data input through a data input pad is transmitted on an input side of a data input circuit to a global write line pair on an output side of the data input circuit during a write operation, and data stored in a memory cell array is transmitted to a local read line pair during a read operation in response to a read column selection signal. In addition, claim 14 is amended herein to clarify that data that is transmitted to the global write line pair is transmitted to a local write line pair in response to a write column selection signal during the write operation, and data that is transmitted to the local read line pair is transmitted to a global read line pair during the read operation. In addition, claim 14 is amended herein to clarify that data that is transmitted to the local write line pair is transmitted to the memory cell array during the write operation, and data that is transmitted to the global read

line pair is transmitted on an input side of a data output circuit to a data output pad on an output side of the data output circuit during the read operation. In addition, claim 14 is amended herein to clarify that the data transmitted through the data input pad and the data transmitted through the data output pad are transmitted simultaneously.

Independent claim 17 is amended herein to clarify that a plurality of write column selection gates of each of the plurality of memory cell array blocks transmits data between a plurality of bit line pairs and a predetermined number of local write line pairs in response to a write column selection signal during a write operation. In addition, claim 17 is amended herein to clarify that read column selection gates of each of the plurality of memory cell array blocks transmits data between the plurality of bit line pairs and a predetermined number of local read line pairs in response to a read column selection signal during a read operation. In addition, claim 17 is amended herein to clarify that a predetermined number of global write line pairs is connected to the predetermined number of local write line pairs of each of the plurality of memory cell array blocks, wherein the predetermined number of global write line pairs receives data input from at least one data input pad. In addition, claim 17 is amended herein to clarify that predetermined number of global read line pairs is connected to the predetermined number of local read line pairs of each of the plurality of memory cell array blocks, wherein the predetermined number of global read line pairs outputs data transmitted from the predetermined number of global read line pairs to at least one data output pad. In addition, claim 17 is amended herein to clarify that the data transmitted from the predetermined number of global read line pairs is received by the at least one data output pad and the data input from at least one data input pad is input through the at least one data input pad simultaneously.

These features as claimed are illustrated by way of example at least at Figures 1 and 3 of the present specification. In this example, data input circuit 16 is between data input pad DQ1 and write line pairs GW1/B - GW4/B, and data output circuit 18 is between data output pad DQ0 and read line pairs GR1/B-GR4/B (see Figure 1 of the present specification). Data input circuit 16 transfers first data DI11-DI14 through data input pad DQ1 to write line pairs LW11/B-LW4/B as second data di1 via global write line pairs GW1/B-GW4/B during a write operation (see Figure 1 and page 14, lines 14-18 of the present specification). Also, during the write

operation, write column decoder 14-2 activates a write column selection signal WY1, wherein write column gates WYG11, WYG12 are turned on, and the second data di1 is transmitted to the local write line pairs LW11/B-LW14/B (see Figures 1 and 3 and page 14, line 21 through page 15, line 3). During a read operation, read column selection gate RYG11 transmits third data do1 to read line pairs LR11/B-LR14/B in response to a read column selection signal RY1 that is generated by read column decoder 14-1 (see Figures 1 and 3 and page 15, paragraph [0035]). Data output circuit 18 outputs the third data do1 as fourth data DO11-DO14 (see Figure 1 and page 14, lines 8-12 of the present specification). The first data DO11-DO14 is input through the data input pad DQ1 during the write operation and the fourth data DI11-DI14 is output through the data output pad 18 during the read operation simultaneously (see Figures 1 and 3 of the present specification).

With regard to amended independent claims 1 and 8, it is submitted that Ooishi fails to teach or suggest a data input circuit that is between at least one data input pad and a predetermined number of write line pairs, as claimed in amended independent claims 1 and 8. In addition, it is submitted that Ooishi fails to teach or suggest a data output circuit between at least one output pad and a predetermined number of read line pairs, as claimed in amended independent claims 1 and 8. Ooishi discloses read data line pairs NRDB, /NRDB and a write data line pairs NWDB, /NWDB (see Ooishi, Figure 4 and column 10, lines 37-39). In addition, Ooishi discloses a circuit between a global data bus GDB and the read write pairs and write line pairs WDBP, which represents the write data line pairs NWDB, /NWDB (see Ooishi, Figures 6-7 and column 12, lines 56-59). While Ooishi also discloses I/O terminals 17 at one end of the global data bus GBD (see Ooishi, Figure 1), there is no teaching or suggestion in Ooishi of a data output circuit between the global data bus GBD or the read data line pair NRDB, /NRDB and the I/O terminals 17 of Ooishi. Nor is there any mention in Ooishi of a data input circuit between the global data bus GBD or the write data line pair NWDB, /NWDB and the I/O terminals 17 of Ooishi.

In addition, with regard to amended independent claims 1, 8, 14, and 17, it is submitted that Ooishi fails to teach or suggest first data which is applied through at least one data input pad during a write operation and fourth data that is output through at least one data output pad during

the read operation simultaneously, as claimed. In particular, Ooishi fails to teach or suggest first data which is applied through at least one data input pad, as claimed, and Ooishi fails to teach or suggest fourth data that is output through at least one data output pad, as claimed, for reasons described above. Moreover, there is no mention in Ooishi of applying first data through the I/O terminals 17 of Ooishi and outputting fourth data through the I/O terminals 17 of Ooishi simultaneously. Rather, Ooishi discloses that multiple memory blocks can be simultaneously activated (see Ooishi, column 6, lines 43-44). Specifically, in Ooishi, reading and writing operations are executed simultaneously in different bank groups (see, for example, Figure 9 which illustrates bank group BG0 and corresponding read signal RBG0 and bank group BG2 and corresponding write signal WBG2 in the same clock cycle) wherein read and write activating signals RDD and WRT are activated within the same clock cycle, and corresponding internal address signals RCAD and WCAD are produced at the same time (see Ooishi, Figure 9, column 14, line 65 through column 15, line 6, and column 16, lines 57-61). In this manner, the read and write operations of Ooishi can be performed in parallel within the same cycle (see Ooishi, Figures 4 and 9 and column 15, lines 10-15). Although Ooishi teaches various signals that are generated during read and write operations in the same clock cycle, this is different than first data being input through a data input pad during a write operation and fourth data being output through a data output pad during a read operation simultaneously (see, for example, Figure 3 and page 14, lines 19-21 of the present specification).

Moreover, as described above, Ooishi teaches terminals 17 (referred to in the Office Action at page 3 as input pads and output pads) that are coupled to the abovementioned global data bus GDB of Ooishi (see Ooishi, Figure 1). Further, the global data bus GDB is divided into a region 98 for transmitting read data and a region 99 for transmitting write data (see Ooishi, Figures 1, 2, and column 7, lines 54-59). However, in Ooishi, read/write data is transmitted between each data line and global data bus regions 98, 99 to terminals 17 via a set of common elements, specifically a single write driver 110, a read amplifier 120, and an interface 130 (see Ooishi, Figure 2 and column 7, line 65 through column 8, line 8). Although the global data bus GDB of Ooishi is partitioned into bus regions to transmit read and write data, respectively, there is no teaching or suggestion of data being input through at least one terminal 17 during a write

operation, and data being output through at least one terminal 17 during a read operation simultaneously, via the single write driver 110, read amplifier 120, and interface 130 of Ooishi. That is, Ooishi cannot perform a data write operation and a data read operation simultaneously, as Applicants claim.

In addition, with regard to amended independent claims 1, 8, 14, and 17, it is submitted that Ooishi fails to teach or suggest a plurality of write column selection gates that transmits data between a plurality of bit line pairs and a predetermined number of write line pairs in response to write column selection signals during a write operation, and Ooishi fails to teach or suggest a plurality of read column selection gates that transmit data between a plurality of bit line pairs and a predetermined number of read line pairs in response to read column selection signals during a read operation, as claimed. Ooishi discloses transistors 2020, 2022 (referred to in the Office Action at page 3 as write column selection gates) that are controlled by sub-write activation lines SWRL0-SWRL3, and transistors 2030, 2032 that are controlled by a write control line signal WCTL (see Ooishi, Figure 4 and column 11, lines 4-15). However, the write control line signal WCTL of Ooishi is not a write column selection signal, but is instead a masking signal for activating transistors 2030, 2032 during a data mask operation (see Ooishi, Figure 4 and column 11, lines 16-19) in which write data is masked and transmission of write data is controlled by the write control signal WCTL.

Ooishi further discloses transistors 2010, 2012 (referred to in the Office Action at page 3 as read column selection gates), the gates of which are connected to sense amplifier nodes of a sense amplifier circuit 230 (see Ooishi, Figure 4 and column 10, lines 64-66). In this manner, transistors 2010, 2012 of Ooishi transmit data of a read sub source line to read data line pair NRDB, /NRDB in response to data of the bit line pair (see Ooishi, Figure 4 and column 11, lines 31-37). However, transistors 2010, 2012 of Ooishi are not Applicants' claimed read column selection gates, since there is no teaching or suggestion of sense amplifier circuit 230 of Ooishi, to which transistors 2010, 2012 are connected, comprising a read column selection signal that is applied to the gates of the transistors 2010, 2012, and therefore, it follows that there is no teaching or suggestion of transistors 2010, 2012 of Ooishi transmitting data between a plurality of bit line pairs and a predetermined number of read line pairs in response to a read column

selection signal during a read operation, as claimed. Accordingly, Ooishi fails to disclose the semiconductor memory device in which the write column selection gate is turned on in response to the write column selection signal to write data, and the read column selection gate is turned on in response to the read column selection signal to transmit data of the bit line pair to the read data line pair. Further, Ooishi fails to disclose at least one data input pad and at least one data output pad which are separated from each other, but instead discloses a global data bus GDB which is separated into a read bus and a write bus, wherein a write driver 110 and interface 130 are commonly connected to the global data bus GDB. Accordingly, the invention of Ooishi cannot perform a data write operation and a data read operation simultaneously.

For these reasons, it is submitted that Ooishi fails to teach the invention set forth in the amended claims. Reconsideration of the rejection of claims 1-3, 11 and 12 under 35 U.S.C. 102(e) based on Ooishi is respectfully requested.

With regard to the rejection of claims 8, 14, 15, and 17 based on the combination of Hidaka and Ooishi, it is submitted that Hidaka, like Ooishi, fails to teach or suggest data transmitted from at least one data input pad that is transmitted during a write operation and data output to at least one data output pad that is output during a read operation simultaneously, as claimed in amended independent claims 8 and 14.

In addition, it is submitted that Hidaka, like Ooishi, fails to teach or suggest that data is received by at least one data output pad and data is input through at least one data input pad simultaneously, as claimed in amended independent claim 17.

In addition, it is submitted that Hidaka, like Ooishi, fails to teach or suggest a plurality of read column selection gates that transmit data between a plurality of bit line pairs and a predetermined number of read line pairs in response to read column selection signals during a read operation, as claimed. Instead, Hidaka discloses read gate circuits RGT1-RGT4 that transmit read column selection signals YRi1-YRi4 to global read data line pairs GRDB, /GRDB in response to bit line pairs BLI, /BL1 through BL4, /BL4, and write column select gates WCSG1-WCSG4 that transmit data on global I/O line pairs GWDB, GWDB to bit line pairs BL1, /BL1 in response to write column select signals YWi1-YWi4 (see Hidaka, Figure 6). This is different than the present invention, which teaches read column selection gates that transmit

data between a plurality of bit line pairs and a predetermined number of read line pairs in response to read column selection signals during a read operation, as claimed. Accordingly, since Hidaka fails to disclose that read gate circuits RGT1-RGT4 of Hidaka are turned on in response to read column selection signals to transmit data of bit line pairs to the read data line pairs GRDB, /GRDB of Hidaka, it follows that the read gate circuits RGT1-RGT4 of Hidaka are not Applicants' claimed read column selection gates.

Since neither Hidaka nor Ooishi teaches or suggests these claimed features, there is no way to combine the references to obtain teaching or suggestion of the claimed features, and therefore, there is no combination of the references that teaches or suggests the invention set forth in the amended claims.

Since Hidaka and Ooishi, taken alone or in combination, fail to teach or suggest the present invention set forth in the amended claims, claims 8, 14, 15, and 17 are believed to be allowable over the cited references. Accordingly, reconsideration of the rejection of claims 8, 14, 15, and 17 under 35 U.S.C. 103(a) based on Hidaka and Ooishi is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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Steven M. Mills
Registration Number 36,610
Attorney for Applicants

Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774
J:\SAM\0536\amendb\amendmentb2.wpd